IN THE CLAIMS:

Please cancel/amend/retain the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a plurality of metal wire patterns which include a fine line pattern having a ~~sub-micron~~ width of less than 1 μm and pad patterns, said plurality of metal wire patterns being formed ~~at~~ by patterning a same ~~pattern~~ layer and being electrically connected to each other, an area of the fine line pattern being formed to be more than 1% of a total area of said plurality of metal wire patterns for preventing corrosion of the fine line pattern from a chemical-mechanical polishing process.

2. (Canceled)

3. (Previously Presented) The semiconductor device as recited in claim 1, wherein the pad patterns include connection pad patterns which electrically connect the pad patterns to the fine line pattern, said connection pad patterns being included in said total area.

4. (Previously Presented) The semiconductor device as recited in claim 1, wherein the plurality of metal wire patterns are made of aluminum or copper.

5. (Currently Amended) A semiconductor device for preventing corrosion of metal wires from a chemical mechanical polishing process, comprising:

a plurality of metal wire patterns which include main fine line patterns having a ~~sub-micron~~ width of less than 1 μm, main pad patterns, and dummy fine line patterns having a sub-micron width, said plurality of metal wire patterns being formed ~~at~~ by patterning a same ~~pattern and~~ layer, an area of the dummy fine line patterns, which are connected to the pad patterns, being formed to be less than 1% of a total area of said plurality of metal wire patterns and also being less than a value obtained by dividing an area of the main fine line patterns by said total area.

6. (Original) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns are formed parallel with the main fine line patterns at a distance of a width of the main fine line pattern.

7. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns are made of aluminum or copper wire.

8. (Previously Presented) The semiconductor device as recited in claim 5, wherein the dummy fine line patterns do not form or contribute to any electric circuit.

9. (Canceled)

10. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include dummy pad pool patterns, to which the dummy fine line patterns are connected, said dummy pad pool patterns and said dummy fine line patterns being electrically disconnected from the main fine line patterns and the main pad patterns.

11. (Canceled).

12. (Previously Presented) The semiconductor device as recited in claim 5, wherein the plurality of metal wire patterns further include connection pad patterns which electrically connect the main pad patterns to the fine line patterns, said connection pad patterns being included in said total area.

13. (Previously Presented) The semiconductor device as recited in claim 12, wherein the total area is represented by Ap+Ac+A+d, where, 'd' represents the area of the dummy fine line patterns, 'Ap' represents an area of the main pad patterns, 'Ac' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.

14. (Canceled).

15. (New) A semiconductor device for preventing corrosion of aluminum or copper wires from a chemical mechanical polishing process, comprising:

a plurality of metal wire patterns which include main fine line patterns having a width of less than 1 μm, main pad patterns, connection pad patterns which electrically connect the main pad patterns to the fine line patterns, and dummy fine line patterns having a sub-micron width, said plurality of metal wire patterns being formed by patterning a same layer, an area of the dummy fine line patterns, which are connected to the pad patterns, being formed to be less than 1% of a total area of said plurality of metal wire patterns according to a formula,

$$(d/(Ap+Ac+A+d) \times 100) < 1\%$$

and also being less than a value obtained by dividing an area of the main fine line patterns by said total area, which is represented by Ap+Ac+A+d, according to a formula,

$$(d/(Ap+Ac+A+d) < A/(Ap+Ac+A+d)$$

where, 'd' represents the area of the dummy fine line patterns, 'Ap' represents an area of the main pad patterns, 'Ac' represents an area of the connection pad patterns and 'A' represents the area of the main fine line patterns.